52. (NEW) Electromagnetic signals propagating on a computer network, comprising:

said electromagnetic signals carrying instruction for the practice of the method of Claim 9 or Claim 46.

53. (NEW) A computer readable media comprising:

said computer readable media containing executable program instruction for the practice of the method of Claim 9 or Claim 46.

REMARKS

This amendment is filed in response to the Final Office Action filed November 18, 2002, and in the Continuing Prosecution Application ("CPA") filed on even date herewith. All objections and rejections are respectfully traversed.

Claims 1-53 are in the case.

Claims 3, 11, 15, 28-37 were amended to better claim the invention.

Claims 22-27 were cancelled without prejudice.

Claims 38-53 were added to better claim the invention.

Claim 3 has been amended to reflect its original form prior to an amendment made on May 21, 2001. Applicants believe that amended claim 3 is in condition for allowance and better claims the invention.

At paragraph 2 of the Final Office Action, the examiner noted that the numbering of claims was not in accordance with 37 C.F.R. § 1.126. Claims 28-37 have been amended to properly number the claims and are presented herein.

At paragraph 3 of the Final Office Action, Claims 29-35 were rejected under 35 U.S.C. § 112, second paragraph.

At paragraph 3(A)(1), claims 30 and 31 were objected to for lacking proper antecedent basis. Amendments to claims 30 and 31 are believed to satisfy this objection.

At paragraph 3(A)(2), claim 32 was objected to for lacking proper antecedent basis. Applicants do not understand this objection as the "said first input register" of claim 32 has antecedent basis in claim 28.

At paragraphs 3(B) and 4, claims 36 and 37 were objected to. As amended, claim 36 teaches "***electromagnetic signals propagating on a computer network comprising: said electromagnetic signals carrying instruction for execution on a processor for performing the method of claim 9.***" Claim 36 is dependent on method claim 9 and properly claims a

signal directed to a practical application of electromagnetic energy. Therefore, claim 36 is a statutory claim as per M.P.E.P. 2106(IV)(B)(1)(c) (". . . a signal claim directed to a practical application of electromagnetic energy is statutory regardless of its transitory nature."). Accordingly, Applicants respectfully urge that claim 36 is in condition for allowance.

Claim 37 teaches "***a computer readable media comprising: said computer readable media containing instruction for execution in a processor for performing the method of claim 9.***" Claim 37 is a proper claim dependent on method claim 9. Furthermore, claim 37 limits the practice of the method of claim 9 to the particular form of "***computer readable media containing instruction for execution in a processor***" directed at the practical application of method claim 9. See In re Beauregard, 53 F.3d 1583 (Fed. Cir. 1995). Accordingly, Applicants respectfully urge that claim 37 is in condition for allowance.

At paragraphs 5, 6 and 7 of the Final Office Action, claims 1-21 were rejected under 35 U.S.C. § 102(e) as being anticipated by Asato, U.S. Patent No. 6,145,074 issued November 7, 2000.

The present invention as set forth in representative claim 1 comprises:

> 1. Apparatus for enabling an instruction to control data flow bypassing hardware within a processor of a programmable processing engine, the apparatus comprising:
>
> a pipeline of the processor, the pipeline having a plurality of stages including instruction decode, writeback and execution stages, the execution stage having a plurality of parallel execution units; and
>
> an instruction set of the processor, the instruction set defining a register decode value, ***that specifies one of a first register decode value which de-***

fines source operand bypassing, and a second register decode value that defines result bypassing from a previous instruction executing in pipeline stages of the processor.

Asato teaches a data processing device that responds to a source operand bypass specification field for bypassing ***an operation result*** prior to writing the result to a register (col. 3, lines 12-22; fig. 1, 5,6; fig. 4, 5,6). Applicants respectfully urge that with respect to the parallel execution units, Asato's disclosure describes only bypasses to pass ***an operation result*** of each slot to a succeeding instruction on the same or a different slot before writing ***the operation result*** to a register. (col. 6, lines 44-56; col. 5, lines 45-52;). Asato describes only ***result bypassing*** as a source operand to a subsequent instruction and therefore does not anticipate the Applicants' invention.

Applicants respectfully urge that Asato does not show Applicants' claimed invention relating to an instruction set ***"that specifies one of a first register decode value which defines source operand bypassing."*** Briefly discussed, Applicants' processor allows bypassing of either an operation result or a ***source operand*** of a preceding instruction from a parallel unit. To take the example from the page 14 of the Application filed September 3, 1999:

(i5) M add R1 ← R2, 5(R3)

(i6) S and R2 ← RISB, R3

In the example, the processor has two parallel units, the M-Unit and the S-Unit. In the above instruction, the M-Unit executes the M add instruction, fetching the displacement operand 5(R3) over the local bus 424. (Application pg. 14; Application fig. 6). Although the S-Unit

has no direct connection to the local bus, the RISB operand in instruction **i6** indicates that the data fetched in the M-Unit from the local bus will be shared with the parallel S-Unit as a source operand through the parallel connection via the multiplexer. The S-Unit lacks direct access to the local bus because encoding a displacement operand requires more bits than possessed by the S-Unit instruction field. (Application pg. 10). Source bypassing enables the parallel S-Unit to use the data transferred over the local bus, while still using fewer bits in the instruction field. The parallel operations envisioned by Asato addresses only bypassing results from a previous instruction to an input of a parallel execution unit. (col. 3, lines 36-67).

Applicants respectfully urge that the Asato patent is legally precluded from anticipating the claimed invention under 35 U.S.C. § 102 because of the absence from the Asato patent of Applicants' instruction set ***"that specifies one of a first register decode value which defines source operand bypassing."***

Please note that independent claims 9, 19 and 28 similarly claim the novel "***source operand bypassing***" aspect of Applicants' invention. New independent claims 40, and 46 also make claims relating to the novel "***source operand bypassing***" of the invention.

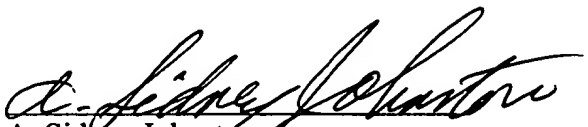
All independent claims are believed to be in condition for allowance.

All dependent claims are believed to be dependent from allowable independent claims, and therefore in condition for allowance.

Favorable action is respectfully solicited.

Please charge any additional fee occasioned by this paper to our Deposit Account No. 03-1237.

Respectfully submitted,



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The replacement for claim 3 resulted from the following changes:

3. The apparatus of Claim [2] 1 wherein the register decode value comprises:

[said second register decode value is] one of a result bypass (RRB) operand and [said first register decode value is] an inter-unit result bypass [(RISB)] (RIRB) operand, each of which explicitly controls data flow within the pipeline of the processor

The replacement for claim 11 resulted from the following changes:

11. (AMENDED) The method of Claim 10 [wherein the] further comprising:

including pipeline stages [include] having instruction decode, writeback and execution stages, and wherein the execution stage [comprises] has multiple parallel execution units including a current execution unit and an alternate execution unit.

The replacement for claim 15 resulted from the following changes:

15. The method of Claim [14] 9 further comprising:

including pipeline stages having instruction decode, writeback and execution stages, and wherein the execution stage has multiple parallel execution units including a current execution unit and an alternate unit; and

sharing source operand data among the parallel execution units of the pipelined processor through the use of a source bypass (RISB) operand in said first register decode value.

The replacement for claim 28 resulted from the following changes:

[26] 28. A processor comprising:

a first execution unit having at least one first input and a first output;

at least one second execution unit having at least one second input and a second output;

a first input register connected to said at least one first input;

a second input register;

a multiplexer having a first input from said first input register, a second input from said second input register, and an output to said at least one second execution unit; and

a register decode value that specifies bypassing data from said first input register to said at least one second execution unit via said multiplexer.

The replacement for claim 29 resulted from the following changes:

[27] 29. The processor of claim [26] 28 further comprising:

a first instruction having at least one first source operand and a first destination, said first execution unit processing said first instruction;

a second instruction having at least one second source operand and a second destination operand, said at least one second source operand is the same as said at least one first source operand; and

means for replacing said at least one second source operand with said register decode value.

The replacement for claim 30 resulted from the following changes:

[28] 30. The processor of claim [27] 29 further comprising:

a register file connected to said first input register and said second input register [registers]; and

means for loading said at least one first and said at least one second source operands from said register file.

The replacement for claim 31 resulted from the following changes:

[29] 31. The processor of claim [27] 29 further comprising:

a memory connected to said first input register [and second input registers]; and

means for loading said at least one first and said at least one second source operands from said memory.

The replacement for claim 32 resulted from the following changes:

[30] 32. The processor of claim [27] 29, said means for replacing further comprising:

an instruction decode mechanism; and

means for said multiplexer choosing input from said first input register.

The replacement for claim 33 resulted from the following changes:

[31] 33. The processor of claim [27] 29 further comprising:

said register decode value having fewer bits than said at least one second source operand.

The replacement for claim 34 resulted from the following changes:

[32] 34. The processor of claim [27] 29 further comprising:

a displacement value within said at least one first and said at least one second source operands, said displacement value specifying an effective memory address where data is stored.

The replacement for claim 35 resulted from the following changes:

[33] 35. The processor of claim [27] 29 further comprising:

a displacement value within said first [and second] destination operand [operands], said displacement value specifying an effective memory address where data is stored.

The replacement for claim 36 resulted from the following changes:

[34] 36. Electromagnetic signals propagating over a computer network[,] comprising:

said electromagnetic signals carrying instruction for execution on a processor [the electromagnetic signals carrying information] for [practicing] performing the method of claim 9.

The replacement for claim 37 resulted from the following changes:

[35] 37. A computer readable media comprising:

said computer readable media containing instruction for execution in a processor for performing the method of claim 9.